

Figure 1 - Examples of Verilog constructs - Prior Art

```
// illustration of Verilog constructs
module verilog_example(out, a, b, reset);
  // Port construct
  output [7:0] out;
  input [7:0] a, b;
  inout reset;

  // Variable construct
  wire internal_reset, q, qn, cp, d, clk;
  reg r1, r2, r3;
  reg [31:0] magic_val;
  reg my_memory [32'hffff, 0];
  integer proc_counter;

  // Parameter construct
  parameter adder_width = 16;

  // Instance constructs
  chip3 arbiter(out, a, b);
  dff1 dff(out[0], qn, cp, d);

  // Gates
  and g1(clk, r1, r2);
  udp3 g2(out[0], qn, cp, d);
  assign (weak0, pull1) #(10, 20, 30) clk = r1 & r2;

  // Scheduled procedural construct
  always @(out[0] or internal_reset)
  begin
    // timing free procedural construct
    r1 = r2;
    magic_val = 0;
    for (proc_counter = 0; proc_counter < adder_width;
        proc_counter = proc_counter + 1)
    begin
      magic_val = magic_val*proc_counte;
    end
    r1 = ^magic_val;
  end

  /* system task construct
  always wait (posedge clk) $display("clk posedge at %t", $time);

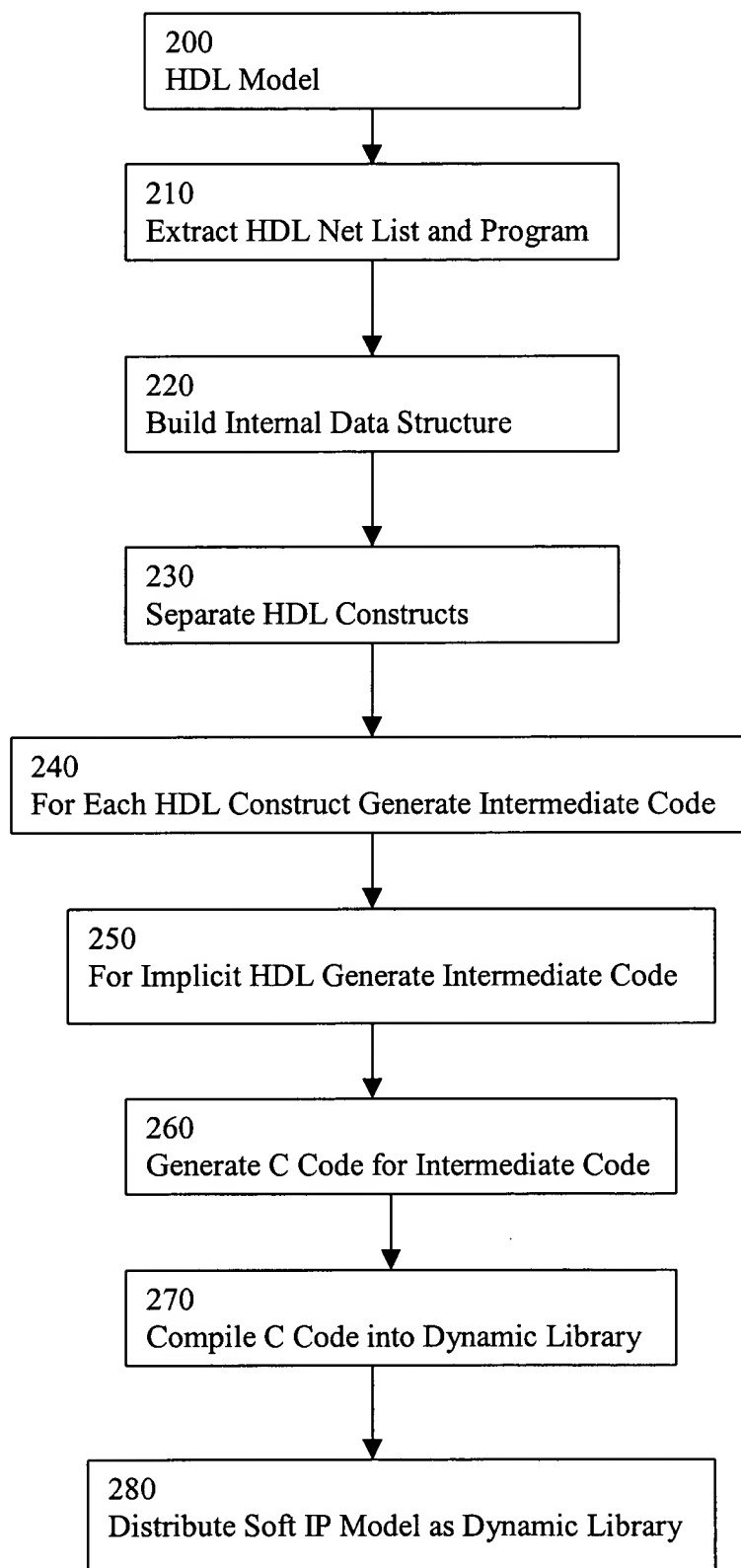
  /* user PLI system task construct */
  initial
  begin
    $pli_init_my_memory(my_memory, 1'bx);
  end

  /* specify path and timing check constructs
  specify
    specparam t0h = 3.0;
    specparam t0l = 5.0;

    (in ==> out[3]) = (t0h, t0h, t0l, t0l, t0l, t0l);
    $setup(posedge clk, d, 4.33, 2.99);
  endspecify

endmodule
```

Fig. 2



300 (Setup)	Add All Soft IP Libraries to PLI Startup Table
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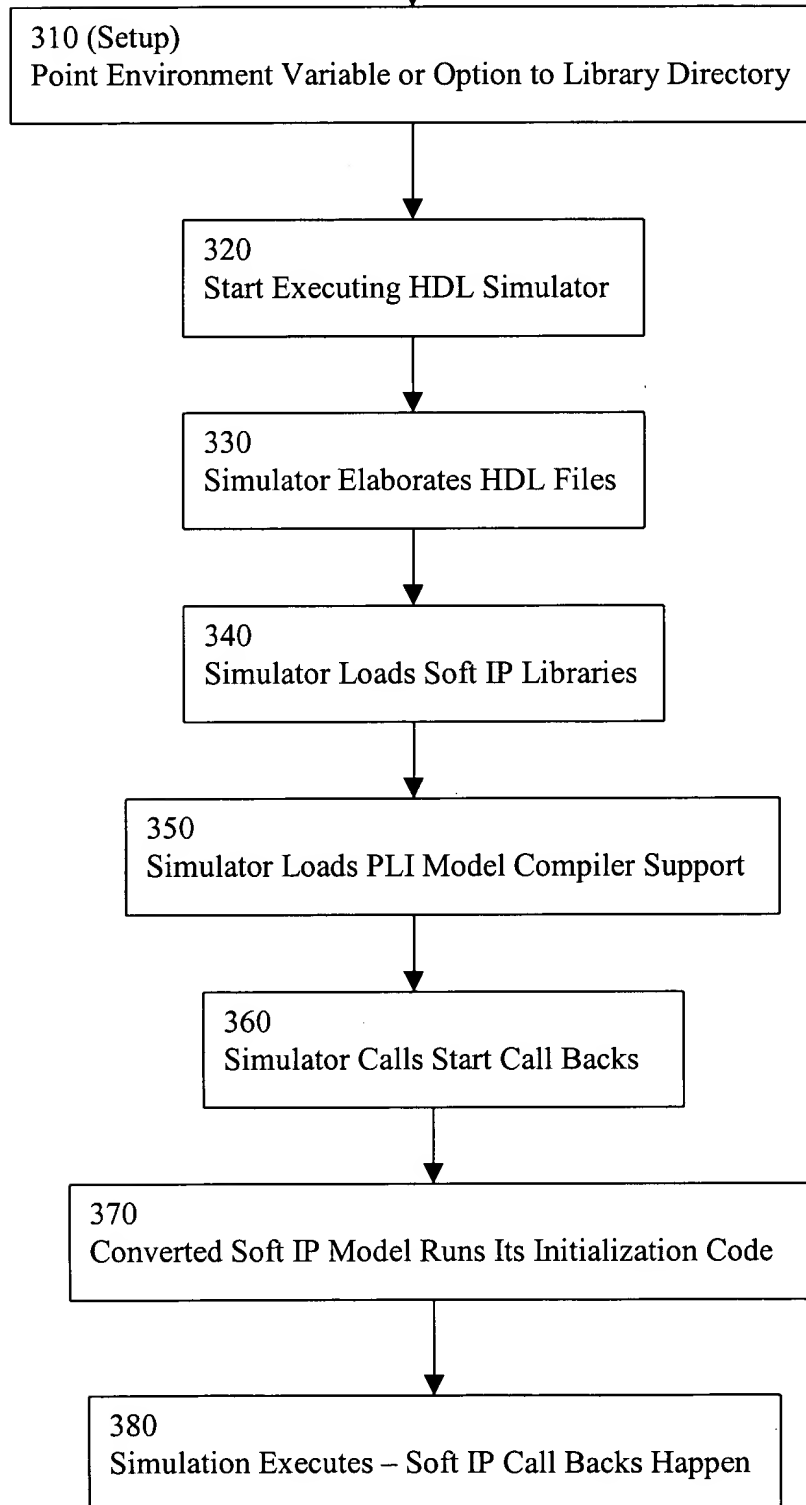


Fig. 4

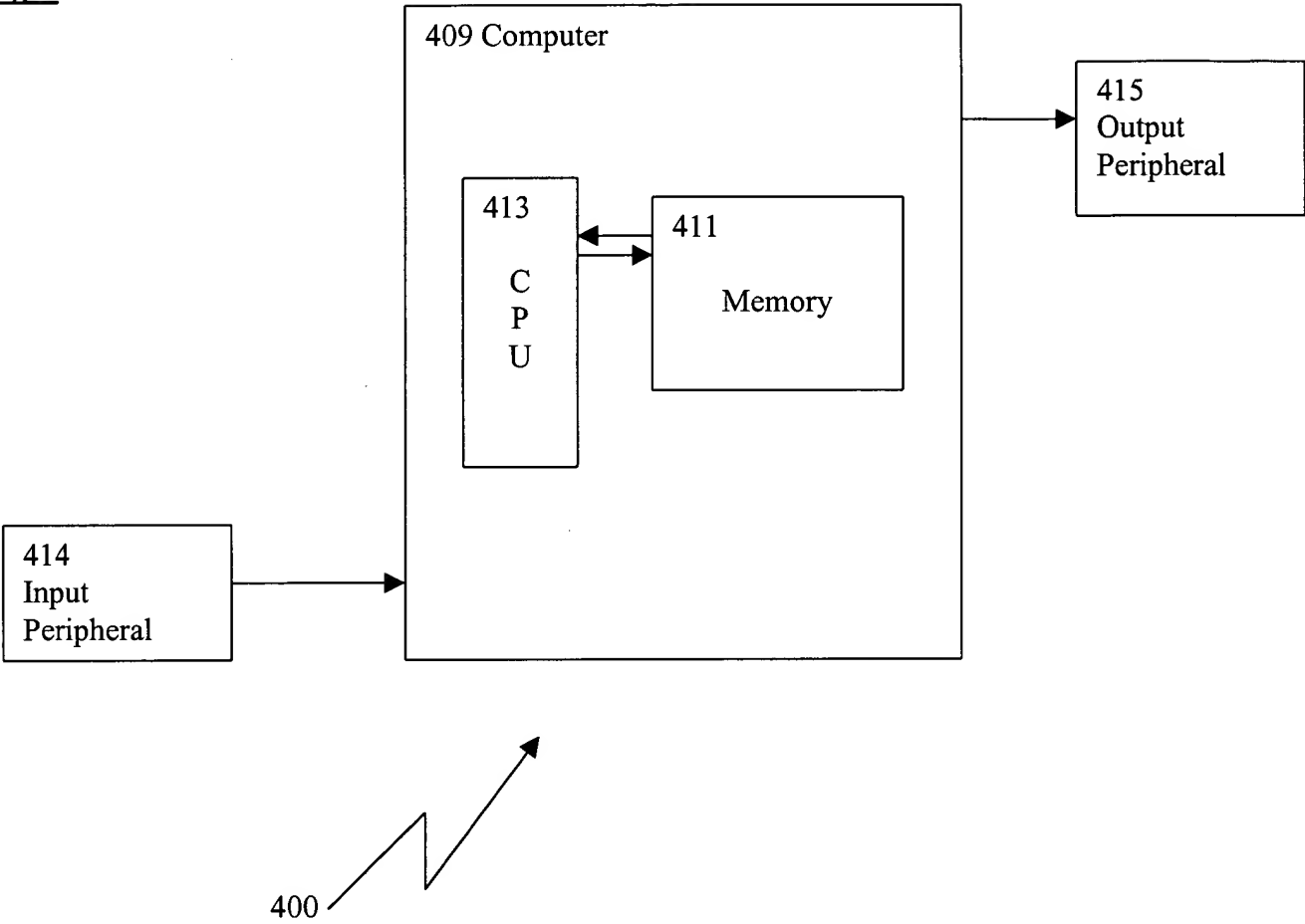
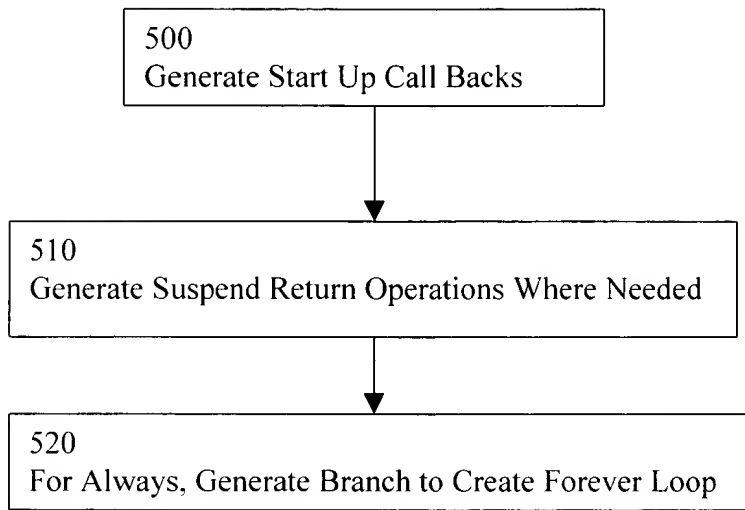


Fig. 5

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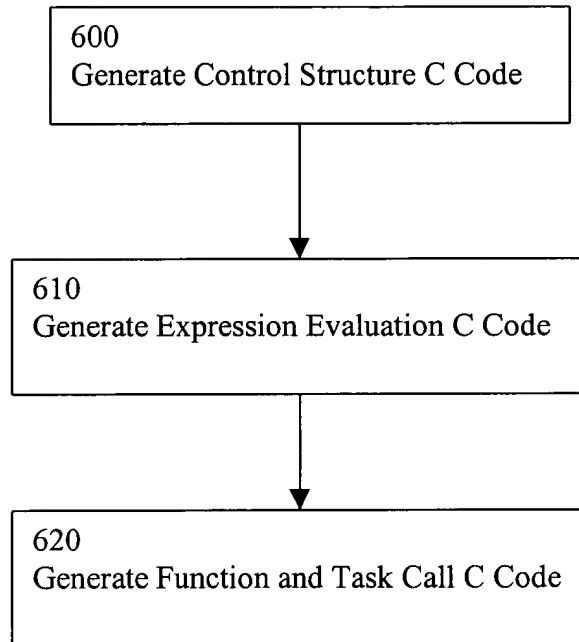
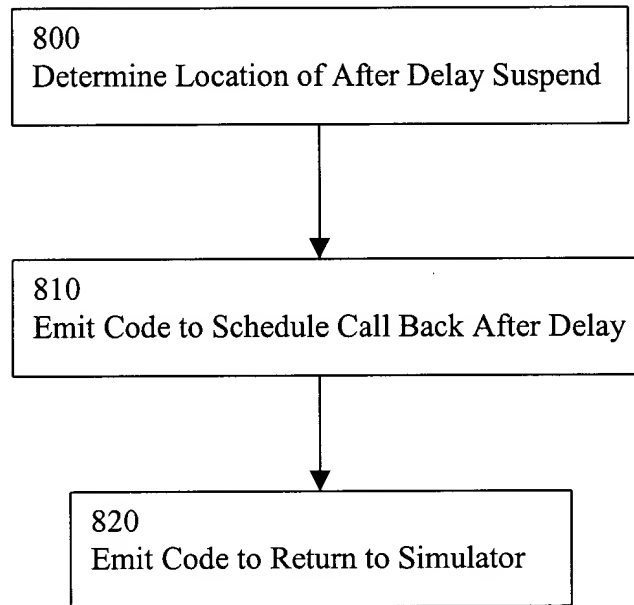
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Fig. 8



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